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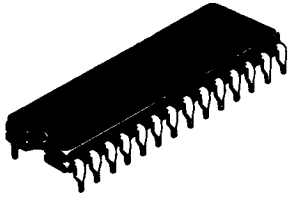
Jameco Part Number 43617

HD6340/HD6840
PTM (Programmable Timer Module)

The HD6340/HD6840 (PTM) is a programmable subsystem component of the HMCS6800 family designed to provide variable system time intervals.

The PTM has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The PTM may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

HD6340P, HD6840P



(DP-28)

The specifications of the HD6340 are for preliminary and may change hereafter.

Please make an inquire at sales office upon adoption of the HD6340.

■ FEATURES

- Operates from a Single 5 volts Power Supply
- Single System Clock Required (E)
- Selectable Prescaler on Timer 3 Capable of 4 MHz for the HD6340/HD6840, 6 MHz for the HD63A40/HD68A40 and 8 MHz for the HD63B40/HD68B40.
- Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- Readable Down Counter Indicates Counts to Go until Time-out
- Selectable Gating for Frequency or Pulse-Width Comparison
- Three Asynchronous External Clock and Gate/Trigger Input Internally Synchronized
- Three Maskable Outputs

– HD6340 –

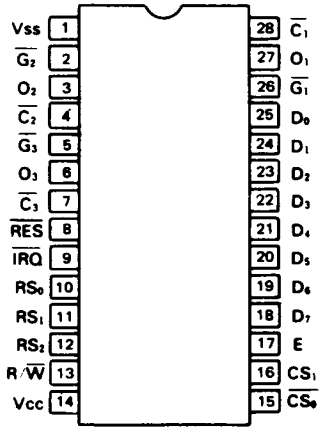
- Wide Range Operating Voltage (V_{CC} = 5V ±10%)
- Low-Power, High-Speed, High-Density CMOS
- Compatible with NMOS PTM (HD6840)

– HD6840 –

- Compatible with MC6840, MC68A40 and MC68B40

■ TYPE OF PRODUCTS

Type	Clock Frequency	Process	Package
HD6340P	1.0 MHz	CMOS	DP-28
HD63A40P	1.5 MHz		
HD63B40P	2.0 MHz		
HD6340FP	1.0 MHz		FP-28
HD63A40FP	1.5 MHz		
HD63B40FP	2.0 MHz		
HD6840P	1.0 MHz	NMOS	DP-28
HD68A40P	1.5 MHz		
HD68B40P	2.0 MHz		
HD6840	1.0 MHz		DC-28
HD68A40	1.5 MHz		
HD68B40	2.0 MHz		



(Top View)

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value		Unit
		HD6340	HD6840	
Supply Voltage	V_{cc}*	−0.3~+7.0	−0.3~+7.0	V
Input Voltage	V_{in}*	−0.3~+7.0	−0.3~+7.0	V
Maximum Output Current	$\|I_o\|$**	10		mA
Operating Temperature	T_{opr}	− 20~+75	− 20~+75	°C
Storage Temperature	T_{stg}	− 55~+150	− 55~+150	°C

* With respect to V_{ss} (SYSTEM GND)

** Maximum output current is the maximum currents which can flow out from one output terminal or I/O common terminal. (D_0 ~ D_7, O_1 ~ O_3, $\overline{IRQ}$)

(NOTE) Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item		Symbol	HD6340			HD6840			Unit
			min	typ	max	min	typ	max	
Supply Voltage		V_{cc}*	4.5	5.0	5.5	4.75	5.0	5.25	V
Input "Low Voltage		V_{IL}*	0	−	0.8	−0.3	−	0.8	V
Input "High" Voltage	E_1 R/$\overline{W}$	V_{IH}*	2.2	−	V_{cc}	2.2	−	V_{cc}	V
	Other Inputs		2.2	−	V_{cc}				
Operating Temperature		T_{opr}	−20	25	75	−20	25	75	°C

* With respect to V_{ss} (SYSTEM GND)

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■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (HD6340; V_{CC} = 5V ±10%, HD6840; V_{CC} = 5V ±5%, V_{SS} = 0V, T_a = −20~+75°C, unless otherwise noted.)

Item	Symbol	HD6340 Test Condition		HD6340 min	HD6340 typ*	HD6340 max	HD6840 Test Condition		HD6840 min	HD6840 typ*	HD6840 max	Unit
Input "High" Voltage	E, R/$\overline{W}$	V_{IH}		2.2	–	V_{CC}	–		2.2	–	V_{CC}	V
	Other Inputs			2.2	–	V_{CC}						
Input "Low" Voltage	V_{IL}			−0.3	–	0.8			−0.3	–	0.8	V
Input Leakage Current	I_{in}	V_{in} = 0 ~ V_{CC} (Except $D_0 \sim D_7$)		−2.5	–	2.5	V_{in}=0~V_{CC} (Except $D_0 \sim D_7$)		−2.5	–	2.5	μA
Three-State Input Current (Off-state)	I_{TSI}	V_{in} = 0.4 ~ V_{CC}, V_{CC} = 5.5V ($D_0 \sim D_7$)		−10	–	10	V_{in} = 0.4~2.4V V_{CC} = 5.25V ($D_0 \sim D_7$)		−10	–	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = −400μA ($D_0 \sim D_7$)		4.1	–	–	I_{LOAD} = −205μA ($D_0 \sim D_7$)		2.4	–	–	V
		$I_{LOAD} \leq$ 10μA ($D_0 \sim D_7$)		V_{CC} −0.1	–	–						
		I_{LOAD} = −400μA (Other Outputs)		4.1	–	–	I_{LOAD} = −200μA ($^{Other}_{Outputs}$)					
		$I_{LOAD} \leq$ 10μA (Other Outputs)		V_{CC}−0.1	–	–						
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6mA ($D_0 \sim D_7$)		–	–	0.4	I_{LOAD} = 1.6mA ($D_0 \sim D_7$)		–	–	0.4	V
		I_{LOAD} = 3.2mA ($O_1 \sim O_3$, $\overline{IRQ}$)					I_{LOAD} = 3.2mA ($O_1 \sim O_3$, $\overline{IRQ}$)					
Output Leakage Current (Off-state)	I_{LOH}	V_{OH} = V_{CC} ($\overline{IRQ}$)		–	–	10	V_{OH} = 2.4V ($\overline{IRQ}$)		–	–	10	μA
Supply Current	I_{CC}	• Chip is not selected. • All counter latches are preset. • $O_1 \sim O_3$ outputs are masked. • Input level (Except E) { V_{IH} min=V_{CC}−0.8V, V_{IL} max = 0.8V	E = 1.0 MHz	–	–	1.0						mA
			E = 1.5 MHz	–	–	1.5						
			E = 2.0 MHz	–	–	2.0						
		• Chip is not selected • Counters are operating. • $O_1 \sim O_3$ operating with load. • Input level (Except E) { V_{IH} min = V_{CC}−0.8, V_{IL} max = 0.8V	E = 1.0 MHz	–	–	3.0						
			E = 1.5 MHz	–	–	4.0						
			E = 2.0 MHz	–	–	6.0						
		• Data bus in R/W operation. • Counters are operating. • $O_1 \sim O_3$ operating with load.	E = 1.0 MHz	–	–	5.0						
			E = 1.5 MHz	–	–	8.0						
			E = 2.0 MHz	–	–	10.0						
Power Dissipation	P_D								–	330	550	mW
Input Capacitance	C_{in}	V_{in} = 0V, T_a = 25°C, f = 1 MHz	$D_0 \sim D_7$	–	–	12.5	V_{in} = 0V, T_a = 25°C, f = 1.0 MHz	$D_0 \sim D_7$	–	–	12.5	pF
			Other Input			7.5		Other Input	–	–	7.5	
Output Capacitance	C_{out}	V_{in} = 0V, T_a = 25°C, f = 1 MHz	$\overline{IRQ}$	–	–	5.0	V_{in} = 0V T_a = 25°C f = 1.0 MHz	$\overline{IRQ}$	–	–	5.0	pF
			O_1, O_2, O_3	–	–	10.0		O_1, O_2, O_3	–	–	10.0	

* T_a = 25°C, V_{CC} = 5.0V

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• AC CHARACTERISTICS (HD6340; V_{CC} = 5V ±10%, HD6840; 5V ±5%, V_{SS} = 0V, T_a = −20~+75°C, unless otherwise noted.)

1. MPU READ TIMING

Item	Symbol	Test Condition	HD6340		HD63A40		HD63B40		HD6840		HD68A40		HD68B40		Unit
			min	max	min	max	min	max	min	max	min	max	min	max	
Enable Cycle Time	t_{cycE}	Fig. 1	1000	10000	666	10000	500	10000	1000	10000	666	10000	500	10000	ns
Enable "High" Pulse Width	PW_{EH}		450	9500	280	9500	220	9500	450	4500	280	4500	220	4500	ns
Enable "Low" Pulse Width	PW_{EL}		430	9500	280	9500	210	9500	430	–	280	–	210	–	ns
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	25	–	25	–	20	–	25	–	25	–	25	ns
Address Set-up Time	t_{AS}		80	–	60	–	40	–	140	–	140	–	70	–	ns
Data Delay Time	t_{DDR}		–	290	–	180	–	150	–	320	–	220	–	180	ns
Data Hold Time	t_{HR}		20	100	20	100	20	100	10	–	10	–	10	–	ns
Address Hold Time	t_{AH}		10	–	10	–	10	–	10	–	10	–	10	–	ns
Data Access Time	t_{ACC}		–	370	–	240	–	190	–	480	–	360	–	250	ns

2. MPU WRITE TIMING

Item	Symbol	Test Condition	HD6340		HD63A40		HD63B40		HD6840		HD68A40		HD68B40		Unit
			min	max	min	max	min	max	min	max	min	max	min	max	
Enable Cycle Time	t_{cycE}	Fig. 2	1000	10000	666	10000	500	10000	1000	10000	666	10000	500	10000	ns
Enable "High" Pulse Width	PW_{EH}		450	9500	280	9500	220	9500	450	4500	280	4500	220	4500	ns
Enable "Low" Pulse Width	PW_{EL}		430	9500	280	9500	210	9500	430	–	280	–	210	–	ns
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	25	–	25	–	20	–	25	–	25	–	25	ns
Address Set-up Time	t_{AS}		80	–	60	–	40	–	140	–	140	–	70	–	ns
Data Set-up Time	t_{DSW}		165	–	80	–	60	–	195	–	80	–	60	–	ns
Data Hold Time	t_{HW}		10	–	10	–	10	–	10	–	10	–	10	–	ns
Address Hold Time	t_{AH}		10	–	10	–	10	–	10	–	10	–	10	–	ns

3 TIMING OF PTM SIGNAL

Item		Symbol	Test Condition	HD6340		HD63A40		HD63B40		HD6840		HD68A40		HD68B40		Unit
				min	max	min	max	min	max	min	max	min	max	min	max	
Input Rise and Fall Time	$\overline{C}$, G, $\overline{RES}$	t_r, t_f	Fig. 3, Fig. 4	–	1000*	–	666*	–	500*	–	1000*	–	666*	–	500*	ns
Input "Low" Pulse Width	$\overline{C}$, G, $\overline{RES}$	PW_L	Fig. 3 Asynchronous Mode	t_{cycE} +tSU +tHD	–	t_{cycE} +tSU +tHD	—	t_{cycE} +tSU +tHD	—	t_{cycE} +tSU +tHD	—	t_{cycE} +tSU +tHD	—	t_{cycE} +tSU +tHD	–	ns
Input "High" Pulse Width	$\overline{C}$, G	PW_H	Fig. 4 Asynchronous Mode	t_{cycE} +tSU +tHD	–	t_{cycE} +tSU +tHD	–	t_{cycE} +tSU +tHD	–	t_{cycE} +tSU +tHD	–	t_{cycE} +tSU +tHD	–	t_{cycE} +tSU +tHD	–	ns
Input Setup Time	$\overline{C}$, G, $\overline{RES}$	t_{SU}	Fig. 5 Synchronous Mode	200	–	120	–	75	–	200	–	120	–	75	–	ns
	$\overline{C_3}$ (÷ 8 Prescaler Mode)			200	–	170	–	170	–	200	–	170	–	170	–	ns
Input Hold Time	$\overline{C}$, G, $\overline{RES}$	t_{HD}	Fig. 5 Synchronous Mode	50	–	50	–	50	–	50	–	50	–	50	–	ns
	$\overline{C_3}$ (÷ 8 Prescaler Mode)			50	–	50	–	50	–	50	–	50	–	50	–	ns
Input Pulse Width	$\overline{C_3}$ (÷ 8 Prescaler Mode)	PW_L PW_H	Asynchronous Mode	120	–	80	–	60	–	125	–	84	–	62.5	–	ns
Output Delay Time	O_1 ~ O_3	t_{co}	Fig. 6	–	200	–	200	–	200	–	700	–	460	–	340	ns
		t_{cm}								–	450	–	450	–	340	ns
		t_{cmos}								–	2000	–	1350	–	1000	ns
Interrupt Release Time		t_{IR}	Fig. 7	–	1200	–	900	–	700	–	1200	–	900	–	700	ns

* t_r, $t_f \leq t_{cycE}$

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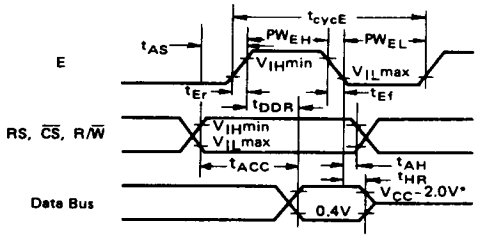

Figure 1 Bus Read Timing
(Read Information from PTM)

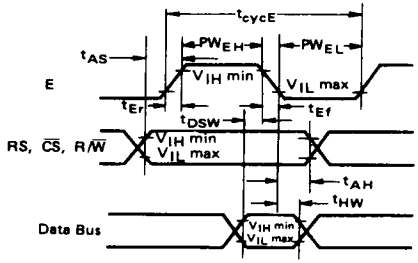

Figure 2 Bus Write Timing
(Write Information into PTM)

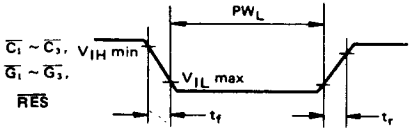

Figure 3 Input Pulse Width "Low"

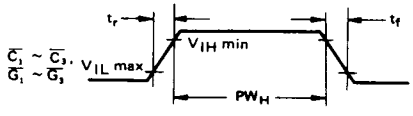

Figure 4 Input Pulse Width "High"

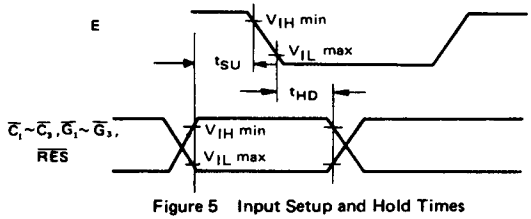

Figure 5 Input Setup and Hold Times

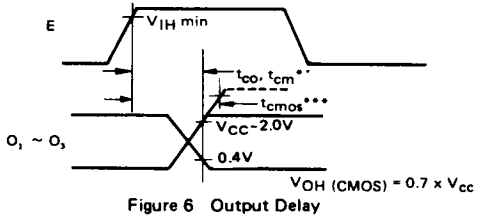

Figure 6 Output Delay

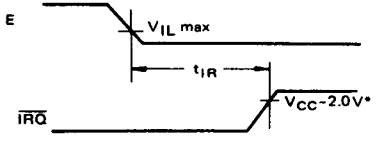

Figure 7 $\overline{IRQ}$ Release Time

* 2.4V for HD6840
, * HD6840 only

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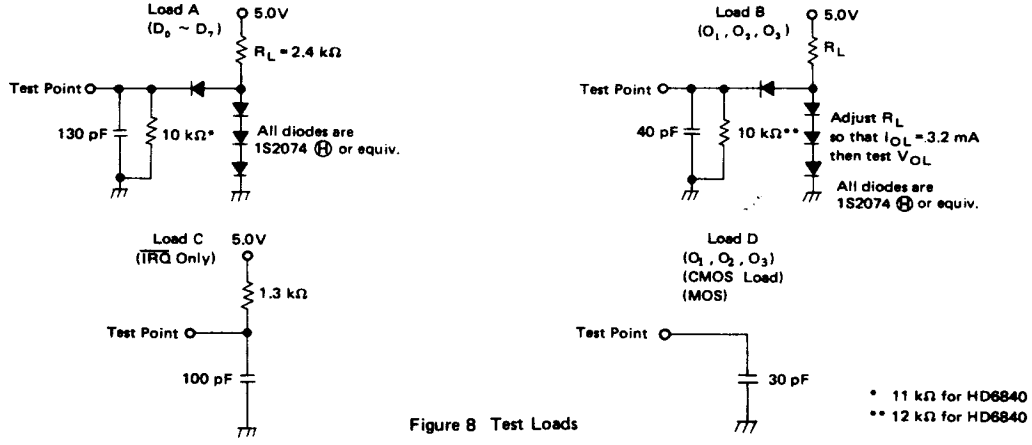

Figure 8 Test Loads

■ GENERAL DESCRIPTION

The PTM is part of the HMCS6800 microprocessor family and is fully bus compatible with HD6800 systems. The three timers in the HD6340/HD6840 operate independently and in several distinct modes to fit a wide variety of measurement and synthesis applications.

The PTM is an integrated set of three distinct counter/timers. It consists of three 16-bit data latches, three 16-bit counters (clocked independently), and the comparison and enable circuitry necessary to implement various measurement and synthesis functions. In addition, it contains interrupt drivers to alert the processor that a particular function has been completed.

In a typical application, a timer will be loaded by first storing two bytes of data into an associated Counter Latch. This data is then transferred into the counter via a Counter initialization cycle. If the counter is enabled, the counter decrements on each subsequent clock period which may be an external clock, or Enable (E) until one of several predetermined conditions causes it to halt or recycle. The timers are thus programmable, cyclic in nature, controllable by external inputs or the MPU program, and accessible by the MPU at any time.

■ PTM INTERFACE SIGNALS FOR MPU

The Programmable Timer Module (PTM) interfaces to the HMCS6800 Bus with an eight-bit bidirectional data bus, two Chip Select lines, a Read/Write line, an Enable (System ϕ_2) line, an Interrupt Request line, an external Reset line, and three Register Select lines. These signals, in conjunction with the HD6800 VMA output, permit the MPU to control the PTM. VMA should be utilized in conjunction with an MPU address line into a Chip Select of the PTM, when the HD6800, HD6802 are used.

- **Bidirectional Data ($D_0 \sim D_7$)**

Input/Output	Pin No. 25 ~ 18

The bidirectional data lines ($D_0 \sim D_7$) allow the transfer of data between the MPU and PTM. The data bus output drivers are three-state devices which remain in the high-impedance (off) state except when the MPU performs a PTM read operation (Read/Write and Enable lines "High" and PTM Chip Selects activated).

- **Chip Select ($\overline{CS_0}$, CS_1)**

Input	Pin No. 15, 16

These two signals are used to activate the Data Bus interface and allow transfer of data from the PTM. With $\overline{CS_0}$ = "Low" and CS_1 = "High", the device is selected and data transfer will occur.

- **Read/Write (R/$\overline{W}$)**

Input	Pin No. 13

This signal is generated by the MPU to control the direction of data transfer on the Data Bus. With the PTM selected, a "Low" state on the PTM R/$\overline{W}$ line enables the input buffers and data is transferred from the MPU to the PTM on the trailing edge of the Enable (System ϕ_2) signal. Alternately, (under the same conditions) R/$\overline{W}$ = "High" and Enable "High" allows data in the PTM to be read by the MPU.

- **Enable (E)**

Input	Pin No. 17

This signal synchronizes data transfer between the MPU and the PTM. It also performs an equivalent synchronization function on the external clock, reset, and gate inputs of the PTM.

- **Interrupt Request ($\overline{IRQ}$)**

Output (open drain)	Pin No. 9

The active "Low" Interrupt Request signal is normally tied directly (or through priority interrupt circuitry) to the $\overline{IRQ}$ input of the MPU. This is an "open drain" output (no load device on the chip) which permits other similar interrupt request lines to be tied together in a wire-OR configuration.

The $\overline{IRQ}$ line is activated if, and only if, the Composite Interrupt Flag (Bit 7 of the Internal Status Register) is asserted. The

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conditions under which the $\overline{IRQ}$ line is activated are discussed in conjunction with the Status Register.

- **Reset ($\overline{RES}$)**

Input	Pin No. 8

A "Low" level at this input is clocked into the PTM by the Enable (System ϕ_2) input. Two Enable pulses are required to synchronize and process the signal. The PTM then recognizes the active "Low" or inactive "High" on the third Enable pulse. If the $\overline{RES}$ signal is asynchronous, an additional Enable period is required if setup times are not met. The $\overline{RES}$ input must be stable "High"/"Low" for the minimum time stated in the AC Characteristics.

Recognition of a "Low" level at this input by the PTM causes the following action to occur:

a. All counter latches are preset to their maximal count values.
b. All Control Register bits are cleared with the exception of CR10 (internal reset bit) which is set.
c. All counters are preset to the contents of the latches.
d. All counter outputs are reset and all counter clocks are disabled.
e. All Status Register bits (interrupt flags) are cleared.

- **Register Select Lines (RS_0, RS_1, RS_2)**

These inputs are used in conjunction with the R/$\overline{W}$ line to select the internal registers, counters and latches as shown in Table 1.

Input	Pin No. 10, 11, 12

It has been previously stated that the PTM is accessed via MPU Load and Store operations in much the same manner as a memory device. The instructions available with the HMCS6800 family of MPUs which perform operations directly on memory should not be used when the PTM is accessed. These instructions actually fetch a byte from memory, perform an operation, then restore it to the same address location. Since the PTM used the R/$\overline{W}$ line as an additional register select input, the modified data may not be restored to the same register if these instructions are used.

■ PTM ASYNCHRONOUS INPUT/OUTPUT SIGNALS

Each of the three timers within the PTM has external clock and gate inputs as well as a counter output line. The inputs are high impedance, TTL compatible lines and outputs are capable of driving two standard TTL loads.

- **Clock Inputs ($\overline{C_1}$, $\overline{C_2}$, $\overline{C_3}$)**

Input	Pin No. 28, 4, 7

Input pins $\overline{C_1}$, $\overline{C_2}$, and $\overline{C_3}$ will accept asynchronous TTL voltage level signals to decrement Timers 1, 2, and 3, respectively. The "High" and "Low" levels of the external clocks must each be stable for at least one system clock period plus the sum

Table 1 Register Selection

Register Select Inputs *			Operations	
RS_2	RS_1	RS_0	R/$\overline{W}$ = "Low"	R/$\overline{W}$ = "High"
L	L	L	$\overline{CR20}$ = "0" Write Control Register #3 CR20 = "1" Write Control Register #1	All bits "0"
L	L	H	Write Control Register #2	Read Status Register
L	H	L	Write MSB Buffer Register	Read Timer #1 Counter
L	H	H	Write Timer #1 Latches	Read LSB Buffer Register
H	L	L	Write MSB Buffer Register	Read Timer #2 Counter
H	L	H	Write Timer #2 Latches	Read LSB Buffer Register
H	H	L	Write MSB Buffer Register	Read Timer #3 Counter
H	H	H	Write Timer #3 Latches	Read LSB Buffer Register

* L; "Low" level, H; "High" level

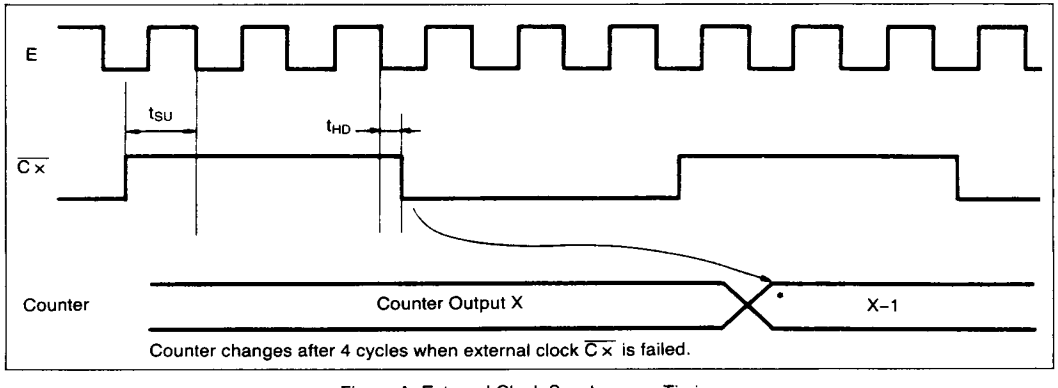

Figure A. External Clock Synchronous Timing

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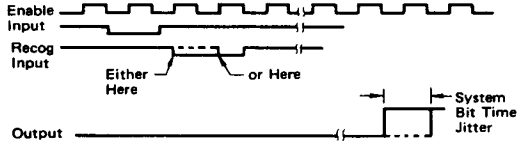
of the setup and hold times for the inputs. The asynchronous clock rate can vary from dc to the limit imposed by Enable (System ϕ_2) Setup, and Hold time.

The external clock inputs are clocked in by Enable (System ϕ_2) pulses. Three Enable periods are used to synchronize and process the external clock. The fourth Enable pulse decrements the internal counter. This does not affect the input frequency, it merely creates a delay between a clock input transition and internal recognition of that transition by the PTM. All references to $\overline{C}$ inputs in this document relate to internal recognition of the input transition. Note that a clock "High" or "Low" level which does not meet setup and hold time specifications may require an additional Enable pulse for recognition. When observing recurring events, a lack of synchronization will result in "jitter" being observed on the output of the PTM when using asynchronous clocks and gate input signals. There are two types of jitter. "System jitter" is the result of the input signals being out of synchronization with the Enable (System ϕ_2), permitting signals with marginal setup and hold time to be recognized by either the bit time nearest the input transition or the subsequent bit time.

"Input jitter" can be as great as the time between input signal negative going transitions plus the system jitter, if the first transition is recognized during one system cycle, and not recognized the next cycle, or vice versa.

External clock input $\overline{C_3}$ represents a special case when Timer #3 is programmed to utilize its optional ÷8 prescaler mode. The maximum input frequency and allowable duty cycles for this case are specified under the AC Characteristics. The output of the ÷8 prescaler is treated in the same manner as the previously discussed clock inputs. That is, it is clocked into the counter by Enable pulses, is recognized on the fourth Enable pulse (provided setup and hold time requirements are met), and must produce an output pulse at least as wide as the sum of an Enable period, setup, and hold times.



- **Gate Inputs ($\overline{G_1}$, $\overline{G_2}$, $\overline{G_3}$)**

Input	Pin No. 26, 2, 5

Input pins $\overline{G_1}$, $\overline{G_2}$, and $\overline{G_3}$ accept asynchronous TTL-compatible signals which are used as triggers or clock gating functions to Timers 1, 2, and 3, respectively. The gating inputs are clocked into the PTM by the Enable (System ϕ_2) signal in the same manner as the previously discussed clock inputs. That is, a $\overline{Gate}$ transition is recognized by the PTM on the fourth Enable pulse (provided setup and hold time requirements are met), and the "High" or "Low" levels of the $\overline{Gate}$ input must be stable for at least one system clock period plus the sum of setup and hold times. All references to $\overline{G}$ transition in this document relate to internal recognition of the input transition.

The $\overline{Gate}$ inputs of all timers directly affected the internal 16-bit counter. The operation of $\overline{G_3}$ is therefore independent of the ÷8 prescaler selection.

- **Timer Outputs (O_1, O_2, O_3)**

Output	Pin No. 27, 3, 6

Timer outputs O_1, O_2, and O_3 are capable of driving up to two TTL loads and produce a defined output waveform for either Continuous or Single-Shot Timer modes. Output waveform definition is accomplished by selecting either Single 16-bit or Dual 8-bit operating modes. The single 16-bit mode will produce a square-wave output in the continuous timer mode and will produce a single pulse in the Single-Shot Timer mode. The Dual 8-bit mode will produce a variable duty cycle pulse in both the continuous and single shot Timer modes. "1" bit of each Control Register (CRX7) is used to enable the corresponding output. If this bit is cleared, the output will remain "Low" (V_{OL}) regardless of the operating mode.

If it is cleared while the output is high the output will go low during the first enable cycle following a write to the Control Register.

The Continuous and Single-Shot Timer Modes are the only ones for which output response is defined in this data sheet. Signals appear at the outputs (unless CRX7 = "0") during Frequency and Pulse Width comparison modes, but the actual waveform is not predictable in typical applications.

■ CONTROL REGISTER

Each timer in the HD6340 has a corresponding write-only Control Register. Control Register #2 has a unique address space (RS0="High", RS1="Low", RS2="Low") and therefore may be written into at any time. The remaining Control Registers (#1 and#3) share the Address Space selected by a "Low" level on all Register Select inputs.

- **CR20**

The least-significant bit of Control Register #2 (CR20) is used as an additional addressing bit for Control Registers #1 and #3. Thus, with all Register selects and R/$\overline{W}$ inputs at "Low" level. Control Register #1 will be written into if CR20 is a logic "1". Under the same conditions, control Register #3 can also be written into after a $\overline{RES}$ "Low" condition has occurred, since all control register bits (except CR10) are cleared. Therefore, one may write in the sequence CR3, CR2, CR1.

- **CR10**

The least-significant bit of Control Register #1 is used as an internal Reset bit. When this bit is a logic "0", all timers are allowed to operate in the modes prescribed by the remaining bits of the control registers. Writing a "1" into CR10 causes all counters to be preset with the contents of the corresponding counter latches, all counter clocks to be disabled, and the timer outputs and interrupt flags (Status Register) to be reset. Counter Latches and Control Registers are undisturbed by an Internal Reset and may be written into regardless of the state of CR10.

- **CR30**

The least-significant bit of Control Register #3 is used as a selector for a ÷8 prescaler which is available with Timer #3 only. The prescaler, if selected, is effectively placed between the clock input circuitry and the input to Counter #3. It can therefore be used with either the internal clock (Enable) or an external clock source.

- **CRX1 ~ CRX7 (X=1~3)**

The functions depicted in the foregoing discussions are tabulated in Table 2 for ease of reference.

Control Register Bits CR10, CR20, and CR30 are unique in that each selects a different function. The remaining bits (1 through 7) of each Control Register select common functions,

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with a particular Control Register affecting only its corresponding timer.

- **CRX1**

Bit 1 of Control Register #1 (CR11) selects whether an internal or external clock source is to be used with Timer #1. Similarly, CR21 selects the clock source for Timer #2, and CR31 performs this function for Timer #3. The function of each bit of Control Register "X" can therefore be defined as shown in the remaining section of Table 2.

- **CRX2**

Control Register Bit 2 selects whether the binary information contained in the Counter Latches (and subsequently loaded into the counter) is to be treated as a single 16-bit word or two 8-bit bytes. In the single 16-bit Counter Mode (CRX2=0) the counter will decrement to zero after N + 1 enabled ($\overline{G}$="Low") clock periods, where N is defined as the 16-bit number in the Counter Latches. With CRX2 = 1, a similar Time Out will occur after (L + 1)·(M + 1) enabled clock periods, where L and M, respectively, refer to the LSB and MSB bytes in the Counter Latches.

- **CRX3 ~ CRX7**

Control Register Bits 3, 4, and 5 are explained in detail in the Timer Operating Mode section. Bit 6 is an interrupt mask bit which will be explained more fully in conjunction with the Status Register, and bit 7 is used to enable the corresponding Timer Output. A summary of the control register programming modes is shown in Table 3.

■ STATUS REGISTER/INTERRUPT FLAGS

The PTM has an internal Read-Only Status Register which contains four Interrupt Flags. (The remaining four bits of the register are not used, and default to "0"s when being read.) Bits 0, 1, and 2 are assigned to Timers 1, 2, and 3, respectively, as individual flag bits, while Bit 7 is a Composite Interrupt Flag. This flag bit will be asserted if any of the individual flag bits is set while Bit 6 of the corresponding Control Register is at a logic "1". The conditions for asserting the Composite Interrupt Flag bit can therefore be expressed as:

$$INT = I_1 \cdot CR16 + I_2 \cdot CR26 + I_3 \cdot CR36$$

where INT = Composite Interrupt Flag (Bit 7)
I_1 = Timer #1 Interrupt Flag (Bit 0)
I_2 = Timer #2 Interrupt Flag (Bit 1)
I_3 = Timer #3 Interrupt Flag (Bit 2)

STATUS REGISTER

7	6	5	4	3	2	1	0
INT					I_3	I_2	I_1

An interrupt flag is cleared by a Timer Reset condition, i.e., External $\overline{RES}$ = "Low" or Internal Reset Bit (CR10) = "1". It will also be cleared by a Read Timer Counter Command provided that the Status Register has previously been read while the interrupt flag was set. This condition on the Read Status Register – Read Timer Counter (RS–RT) sequence is designed to prevent missing interrupts which might occur after the status register is read, but prior to reading the Timer Counter.

An Individual Interrupt Flag is also cleared by a Write Timer Latches (W) command or a Counter Initialization (CI) sequence, provided that W or CI affects the Timer corresponding to the individual Interrupt Flag.

Table 2 Control Register Bits

CONTROL REGISTER #1		CONTROL REGISTER #2		CONTROL REGISTER #3	
CR10	Internal Reset Bit	CR20	Control Register Address Bit	CR30	Timer #3 Clock Control
"0" All timers allowed to operate "1" All timers held in preset state		"0" CR #3 may be written "1" CR #1 may be written		"0" T3 Clock is not prescaled "1" T3 Clock is prescaled by ÷ 8	
CRX1*		Timer #X Clock Source			
"0"		TX uses external clock source on $\overline{CX}$ input			
"1"		TX uses Enable clock			
CRX2		Timer #X Counting Mode Control			
"0"		TX configured for normal (16-bit) counting mode			
"1"		TX configured for dual 8-bit counting mode			
CRX3 CRX4 CRX5		Timer #X Counter Mode and Interrupt Control (See Table 3)			
CRX6		Timer #X Interrupt Enable			
"0"		Interrupt Flag masked on $\overline{IRQ}$			
"1"		Interrupt Flag enabled to $\overline{IRQ}$			
CRX7		Timer #X Counter Output Enable			
"0"		TX Output masked on output OX			
"1"		TX Output enabled on output OX			

* Control Register for Timer 1, 2, or 3, Bit 1.

■ COUNTER LATCH INITIALIZATION

Each of the three independent timers consists of a 16-bit addressable counter and 16 bits of addressable latches. The counters are preset to the binary numbers stored in the latches. Counter initialization results in the transfer of the latch contents to the counter. See notes in Table 5 regarding the binary number N, L, or M placed into the Latches and their relationship to the output waveforms and counter Time-Outs.

Since the PTM data bus is 8-bits wide and the counters are 16-bits wide, a temporary register (MSB Buffer Register) is provided. This "write only" register is for the Most Significant Byte of the desired latch data. Three addresses are provided for the MSB Buffer Register (as indicated in Table 1), but they all lead to the same Buffer. Data from the MSB Buffer will automatically be transferred into the Most Significant Byte of Timer #X when a Write Timer #X Latches Command is performed. So it can be seen that the PTM has been designed to allow transfer of two bytes of data into the counter latches provided that the MSB is transferred first.

In many applications, the source of the data will be as

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HMCS6800 MPU. It should be noted that the 16-bit store operations of the HMCS6800 microprocessors (STS and STX etc.) transfer data in the order required by the PTM. A Store Index Register Instruction, for example, results in the MSB of the X register being transferred to the selected address, then the LSB of the X register being written into the next higher location. Thus, either the index register or stack pointer may be transfered directly into a selected counter latch with a single instruction.

A logic "Low" at the $\overline{RES}$ input also initializes the counter latches. In this case, all latches will assume a maximum count of $(65,536)_{10}$. It is important to note that an Internal Reset (Bit 0 of Control Register 1 Set) has no effect on the counter latches.

■ COUNTER INITIALIZATION

Counter Initialization is defined as the transfer of data from the latches to the counter with subsequent clearing of the Individual Interrupt Flag associated with the counter. Counter Initialization always occurs when a reset condition ($\overline{RES}$ = "Low" or CR10 = "1") is recognized. It can also occur – depending on Timer Mode – with a Write Timer Latches command or recognition of a negative transition of the $\overline{Gate}$ input.

Counter recycling or re-initialization occurs when a negative transition of the clock input is recognized after the counter has reached an all-zero state. In this case, data is transferred from the Latches to the Counter.

■ TIMER OPERATING MODES

The PTM has been designed to operate effectively in a wide variety of applications. This is accomplished by using three bits of each control register (CRX3, CRX4, and CRX5) to defined different operating modes of the Timers. These modes are divided into Wave Synthesis and Wave Measurement modes, and outlined in Table 3.

One of the WAVE SYNTHESIS modes is the Continuous Operating mode, which is useful for cyclic wave generation. Either symmetrical or variable duty-cycle waves can be generated in this mode. The other wave synthesis mode, the Single-Shot mode, is similar in use to the Continuous operating mode, however, a single pulse is generated, with a programmable preset width.

The WAVE MEASUREMENT modes include the Frequency Comparison and Pulse Width Comparison modes which are used to measure cyclic and singular pulse widths, respectively.

In addition to the four timer modes in Table 3, the remaining control register bit is used to modify counter initialization and enabling or interrupt conditions.

■ WAVE SYNTHESIS MODES

• Continuous Operating Mode (Table 4)

The continuous mode will synthesize a continuous wave with a period proportional to the preset number in the particular timer latches.

Any of the timers in the PTM may be programmed to operate in a continuous mode by writing "0"s into bits 3 and 5 of the corresponding control register. Assuming that the timer output is enabled (CRX7 = "1"), either a square wave or a variable duty cycle waveform will be generated at the Timer Output, OX. The type of output is selected via Control Register Bit 2.

Either a Timer Reset (CR10 = "1" or External $\overline{RES}$ = "Low") condition or internal recognition of a negative transition of the $\overline{Gate}$ input results in Counter Initialization. A Write Timer Latches command can be selected as a Counter Initialization signal by clearing CRX4.

The counter is enabled by an absence of a Timer Reset condition and a "Low" level at the $\overline{Gate}$ input. In the 16-bit mode, the counter will decrement on the first clock cycle during or after the counter initialization cycle. It continues to decrement on each clock signal so long as $\overline{G}$ remains "Low" and no reset condition exists. A Counter Time Out (the first clock after all

Table 3 Operating Modes

Control Register			Timer Operating Mode	
CRX3	CRX4	CRX5		
0	*	0	Continuous	Wave Synthesis
0	*	1	Single-Shot	
1	0	*	Frequency Comparison	Wave Measurement
1	1	*	Pulse Width Comparison	

* Defines Additional Timer Functions.

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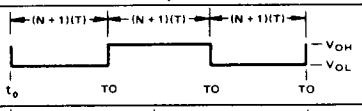
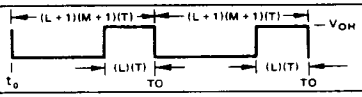
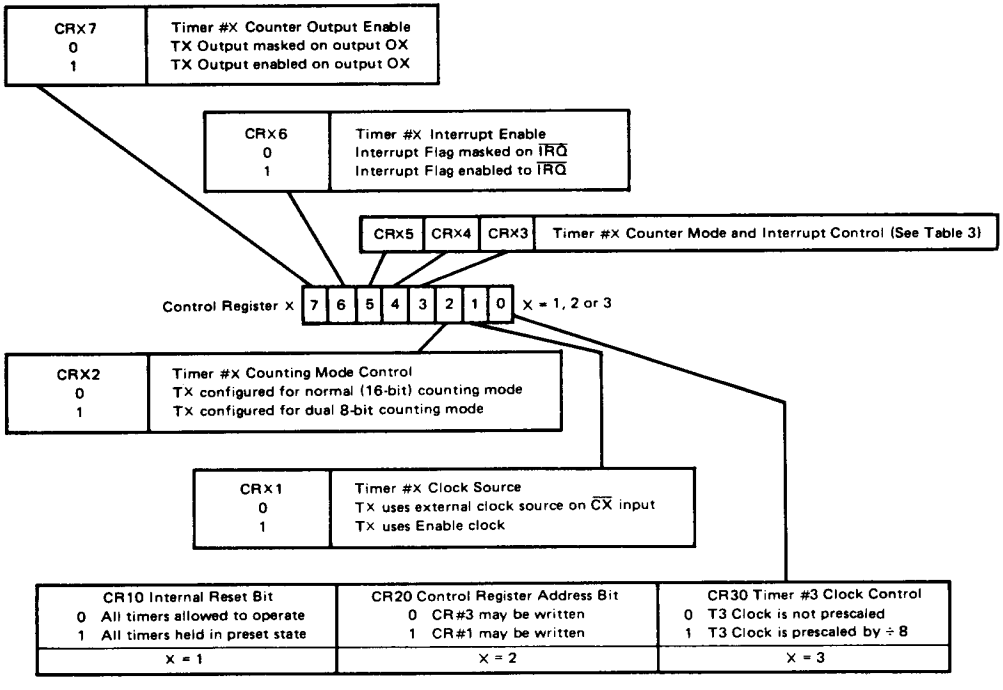
Table 4 Continuous Operating Modes

CONTINUOUS MODE (CRX3 = "0", CRX5 = "0")			
Control Register		**Initialization/Output Waveforms**	
CRX2	**CRX4**	**Counter Initialization**	***Timer Output (OX) (CRX7 = "1")**
0	0	$\overline{G}\downarrow$+W+R	
0	1	$\overline{G}\downarrow$+R	
1	0	$\overline{G}\downarrow$+W+R	
1	1	$\overline{G}\downarrow$+R	

$\overline{G}\downarrow$ = Negative transition of $\overline{\text{Gate}}$ input.
W = Write Timer Latches Command.
R = Timer Reset (CR10 = "1" or External $\overline{\text{RES}}$ = "Low")
N = 16-Bit Number in Counter Latch.
L = 8-Bit Number in LSB Counter Latch.
M = 8-Bit Number in MSB Counter Latch.
T = Clock Input Negative Transitions to Counter.
t_0 = Counter Initialization Cycle.
TO = Counter Time Out (All Zero Condition).

* All time intervals shown above assume the $\overline{\text{Gate}}$ ($\overline{G}$) and $\overline{\text{Clock}}$ ($\overline{C}$) signals are synchronized to Enable (System ϕ_2) with the specified setup and hold time requirements.

Control Register Bits



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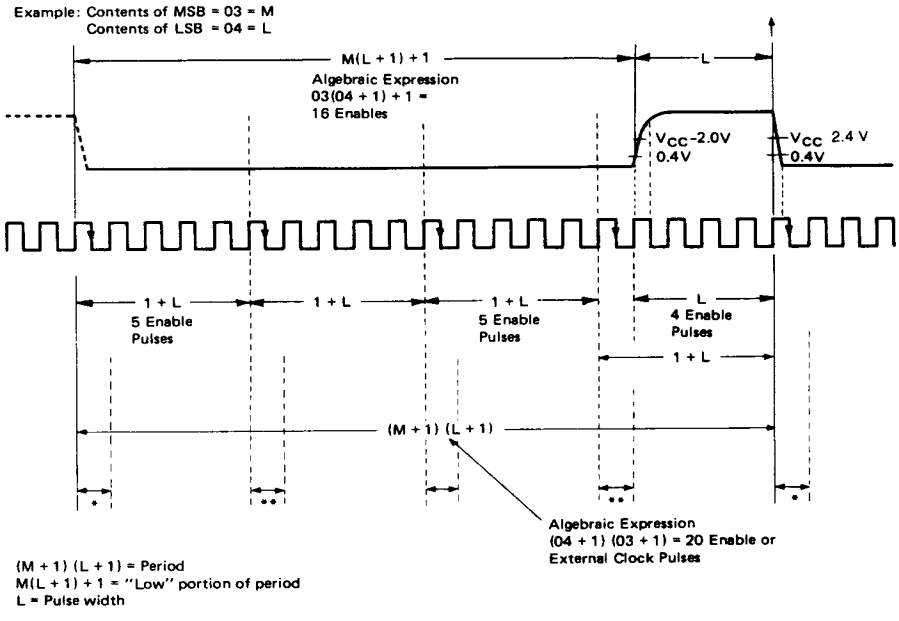

* Preset LSB and MSB to Respective Latches on the negative transition of the E.
** Preset LSB to LSB Latches and Decrement MSB by one on the negative transition of the E.

Figure 9 Timer Output Waveform Example
(Continuous Dual 8-Bit Mode using Internal Enable)

counter bits = "0") results in the Individual Interrupt Flag being set and re-initialization of the counter.

In the dual 8-bit mode (CRX2= "1") [Refer to the example in Fig. 9] the MSB decrements once for every full countdown of the LSB + 1. When the LSB = "0", the MSB is unchanged; on the next clock pulse the LSB is reset to the count in the LSB Latches and the MSB is decremented by 1 (one). The output, if enabled, remains "Low" during and after initialization and will remain "Low" until the counter MSB is all "0"s. The output will go "High" at the beginning of the next clock pulse. The output remains "High" until both the LSB and MSB of the counter are all "0"s. At the beginning of the next clock pulse the defined Time Out (TO) will occur and the output will go "Low". In the Dual 8-bit mode the period of the output of the example in Fig. 9 would span 20 clock pulses as opposed to the 1546 clock pulses using the Normal 16-bit mode.

A special time-out condition exists for the dual 8-bit mode (CRX2 = "1") if L = "0". In this case, the counter will revert to a mode similar to the single 16-bit mode, except Time Out occurs after M+1 clock pulses. The output, if enabled, goes "Low" during the Counter Initialization cycle and reverses state at each Time Out. The counter remains cyclical (is re-initialized at each Time Out) and the Individual Interrupt Flag is set when Time Out occurs. If M = L = "0", the internal counters do not change, but the output toggles at a rate of 1/2 the clock frequency.

The discussion of the Continuous Mode has assumed that the application requires an output signal. It should be noted that the Timer operates in the same manner with the output disabled (CRX7 = "0"). A Read Timer Counter command is valid regardless of the state of CRX7.

- **Single-Shot Timer Mode**

This mode is identical to the Continuous Mode with three exceptions. The first of these is obvious from the name – the output returns to a "Low" level after the initial Time Out and remains "Low" until another Counter Initialization cycle occurs. The waveforms available are shown in Table 5.

As indicated in Table 5, the internal counting mechanism remains cyclical in the Single-Shot Mode. Each Time Out of the counter results in the setting of an Individual Interrupt Flag and re-initialization of the counter.

The second major difference between the Single-Shot and Continuous modes is that the internal counter enable is not dependent on the $\overline{\text{Gate}}$ input level remaining in the "Low" state for the Single-Shot mode.

Another special condition is introduced in the Single-Shot mode. If L = M = "0"(Dual 8-bit) or N = "0" (Single 16-bit), the output goes "Low" on the first clock received during or after Counter Initialization. The output remains "Low" until the Operating Mode is changed or nonzero data is written into the Counter Latches. Time Outs continue to occur at the end of each clock period.

The three differences between Single-Shot and Continuous Timer Modes can be summarized as attributes of the Single-Shot

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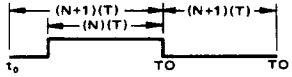
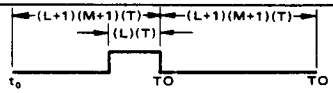
mode:

1. Output is enabled for only one pulse until it is reinitialized.
2. Counter Enable is independent of $\overline{Gate}$.
3. L = M = "0" or N = "0" disables output.

Aside from these differences, the two modes are identical.

Table 5 Single-Shot Operating Modes

Single-Shot Mode (CRX3 = "0", CRX7 = "1", CRX5 = "1")			
Control Register		Initialization/Output Waveforms	
CRX2	CRX4	Counter Initialization	Timer Output (OX)
0	0	$\overline{G}\downarrow$+W+R	
0	1	$\overline{G}\downarrow$+R	
1	0	$\overline{G}\downarrow$+W+R	
1	1	$\overline{G}\downarrow$+R	

Symbols are as defined in Table 5.

■ WAVE MEASUREMENT MODES

The Wave Measurement Modes are the Frequency (period) Measurement and Pulse Width Comparison Modes, and are provided for those applications which require more flexibility of interrupt generation and Counter Initialization. Individual Interrupt Flags are set in these modes as a function of both Counter Time Out and transitions of the $\overline{Gate}$ input. Counter Initialization is also affected by Interrupt Flag status.

A timer's output is normally not used in a Wave Measurement mode, but it is defined. If the output is enabled, it will operate as follows. During the period between reinitialization of the timer and the first Time Out, the output will be a logical zero. If the first Time Out is completed (regardless of its method of generation), the output will go "High". If further TO's occur, the output will change state at each completion of a Time-Out.

The counter does operate in either Single 16-bit or Dual 8-bit modes as programmed by CRX2. Other features of the Wave Measurement Modes are outlined in Table 6.

Table 6 Wave Measurement Modes

CRX3 = "1"			
CRX4	CRX5	Application	Condition for Setting Individual Interrupt Flag
0	0	Frequency Comparison	Interrupt Generated if $\overline{Gate}$ Input Period (1/F) is less than Counter Time Out (TO)
0	1	Frequency Comparison	Interrupt Generated if $\overline{Gate}$ Input Period (1/F) is greater than Counter Time Out (TO)
1	0	Pulse Width Comparison	Interrupt Generated if $\overline{Gate}$ Input "Down Time" is less than Counter Time Out (TO)
1	1	Pulse Width Comparison	Interrupt Generated if $\overline{Gate}$ Input "Down Time" is greater than Counter Time Out (TO)

• Frequency Comparison or Period Measurement Mode (CRX3 = "1", CRX4 = "0")

The Frequency Comparison Mode with CRX5 = "1" is straightforward. If Time Out occurs prior to the first negative transition of the $\overline{Gate}$ input after a Counter Initialization cycle, an Individual Interrupt Flag is set. The counter is disabled, and a Counter Initialization cycle cannot begin until the interrupt flag is cleared and a negative transition on $\overline{G}$ is detected.

If CRX5 = "0", as shown in Table 6 and Table 7, an interrupt is generated if $\overline{Gate}$ input returns "Low" prior to a Time Out. If Counter Time-Out occurs first, the counter is recycled and continues to decrement. A bit is set within the timer on the initial Time Out which precludes further individual interrupt generation until a new Counter Initialization cycle has been completed. When this internal bit is set, a negative transition of the $\overline{Gate}$ input starts a new Counter Initialization cycle. (The condition of $\overline{G}\downarrow \cdot \overline{I} \cdot TO$ is satisfied, since a Time Out has occurred and no individual Interrupt has been generated.)

Any of the timers within the PTM may be programmed to compare the period of a pulse (giving the frequency after calculations) at the Gate input with the time period requested for Counter Time-Out. A negative transition of the $\overline{Gate}$ input enables the counter and starts a Counter Initialization cycle – provided that other conditions as noted in Table 7 are satisfied. The counter decrements on each clock signal recognized during or after Counter Initialization until an Interrupt is generated, a Write Timer Latches command is issued, or a Timer Reset condition occurs. It can be seen from Table 7 that an interrupt condition will be generated if CRX5 = "0" and the period of the pulse (single pulse or measured separately repetitive pulses) at the $\overline{Gate}$ input is less than the Counter Time Out period. If CRX5 = "1", an interrupt is generated if the reverse is true.

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Assume now with CRX5 = "1" that a Counter Initialization has occurred and that the $\overline{Gate}$ input has returned "Low" prior to Counter Time Out. Since there is no Individual Interrupt Flag generated, this automatically starts a new Counter Initialization Cycle. The process will continue with frequency comparison being performed on each $\overline{Gate}$ input cycle until the mode is changed, or a cycle is determined to be above the predetermined limit.

- **Pulse Width Comparison Mode (CRX3 = "1", CRX4 = "1")**

This mode is similar to the Frequency Comparison Mode except for a positive, rather than negative, transition of the $\overline{Gate}$ input terminates the count. With CRX5 = "0", an Individual Interrupt Flag will be generated if the "Low" level pulse applied to the $\overline{Gate}$ input is less than the time period required for Counter Time Out. With CRX5 = "1", the interrupt is generated when the reverse condition is true.

As can be seen in Table 8, a positive transition of the $\overline{Gate}$ input disables the counter. With CRX5 = "0", it is therefore possible to directly obtain the width of any pulse causing an interrupt. Similar data for other Time Interval Modes and conditions can be obtained, if two sections of the PTM are dedicated to the purpose.

Table 7 Frequency Comparison Mode

CRX3 = "1", CRX4 = "0"				
Control Reg Bit 5 (CRX5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (I)
0	$\overline{G}\downarrow\cdot\overline{T}\cdot(\overline{CE}+TO)+R$	$\overline{G}\downarrow\cdot\overline{W}\cdot\overline{R}\cdot\overline{T}$	W+R+I	$\overline{G}\downarrow$ Before TO
1	$\overline{G}\downarrow\cdot\overline{T}+R$	$\overline{G}\downarrow\cdot\overline{W}\cdot\overline{R}\cdot\overline{T}$	W+R+I	TO Before $\overline{G}\downarrow$

I represents the interrupt for a given timer.

Table 8 Pulse Width Comparison Mode

CRX3 = "1", CRX4 = "1"				
Control Reg Bit 5 (CRX5)	Counter Initialization	Counter Enable Flip-Flop Set (CE)	Counter Enable Flip-Flop Reset (CE)	Interrupt Flag Set (I)
0	$\overline{G}\downarrow\cdot\overline{T}+R$	$\overline{G}\downarrow\cdot\overline{W}\cdot\overline{R}\cdot\overline{T}$	W+R+I+G	$\overline{G}\uparrow$ Before TO
1	$\overline{G}\downarrow\cdot\overline{T}+R$	$\overline{G}\downarrow\cdot\overline{W}\cdot\overline{R}\cdot\overline{T}$	W+R+I+G	TO Before $\overline{G}\uparrow$

G = Level sensitive recognition of $\overline{Gate}$ input.

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Table 9 Control Register Programming

7	6	5	4	3	2	1	0		Register 1	Register 2	Register 3
X	X	X	X	X	X	X	‡	"0"	All Timers Operate	Reg #3 May Be Written	T3 Clk ÷ 1
								"1"	All Timers Preset	Reg #1 May Be Written	T3 Clk ÷ 8

7	6	5	4	3	2	1	0		
X	X	X	X	X	X	‡	X	"0"	External Clock ($\overline{CX}$ Input)
								"1"	Internal Clock (Enable)

7	6	5	4	3	2	1	0		
X	X	X	X	X	‡	X	X	"0"	Normal (16-Bit) Count Mode
								"1"	Dual 8-Bit Count Mode

7	6	5	4	3	2	1	0	
X	X	0	0	0	X	X	X	Continuous Operating Mode: $\overline{Gate}$ ↓ or Write to Latches or Reset Causes Counter Initialization
X	X	0	0	1	X	X	X	Frequency Comparison Mode: Interrupt if $\overline{Gate}$ is < Counter Time Out
X	X	0	1	0	X	X	X	Continuous Operating Mode: $\overline{Gate}$ ↓ or Reset Causes Counter Initialization
X	X	0	1	1	X	X	X	Pulse Width Comparison Mode: Interrupt if $\overline{Gate}$ is < Counter Time Out
1	X	1	0	0	X	X	X	Single Shot Mode: $\overline{Gate}$ ↓ or Write to Latches or Reset Causes Counter Initialization
X	X	1	0	1	X	X	X	Frequency Comparison Mode: Interrupt If $\overline{Gate}$ is > Counter Time Out
1	X	1	1	0	X	X	X	Single Shot Mode: $\overline{Gate}$ ↓ or Reset Causes Counter Initialization
X	X	1	1	1	X	X	X	Pulse Width Comparison Mode: Interrupt If $\overline{Gate}$ is > Counter Time Out

7	6	5	4	3	2	1	0		
X	‡	X	X	X	X	X	X	"0"	Interrupt Flag Masked ($\overline{IRQ}$)
								"1"	Interrupt Flag Enabled ($\overline{IRQ}$)

7	6	5	4	3	2	1	0		
‡	X	X	X	X	X	X	X	"0"	Timer Output Masked
								"1"	Timer Output Enable

(NOTE) Reset is Hardware or Software Reset ($\overline{RES}$ = "Low" or CR10 = "1").

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■ **NOTE FOR USE (HD6340 only)**

Input signal, which is not necessary for user's application, should be used fixed to "High" or "Low" level. This is applicable to the following signal pins.

$\overline{C_1}, \overline{C_2}, \overline{C_3}, \overline{G_1}, \overline{G_2}, \overline{G_3}$

■ **RESTRICTION FOR USE**

● **Notes for the $O_1 - O_3$ Outputs Noise**

(1) Phenomenon

When the excessive load capacitance is connected to data bus and GND wiring impedance is not neglectable in the system using HD6340, the noise appears in $O_1 - O_3$ outpus in the read cycle as indicated in Fig. 10 which may cause the erroneous operation of the system.

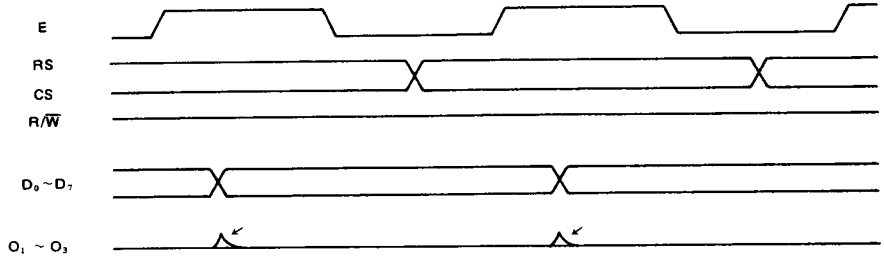


Figure 10 The $O_1 - O_3$ Outputs Noise in the MPU Read Cycle

(2) Cause

When the data buffer turns from "H" to "L", the excessive transient current runs to the GND (the discharge current of the data bus load capacity). Therefore, the noise occurs in the GND pin of the LSI because of the impedance of the GND wiring (resistance and inductance). See Fig. 11 for the details.

Fig. 12 indicates the dependence of the noise voltage upon each parameter.

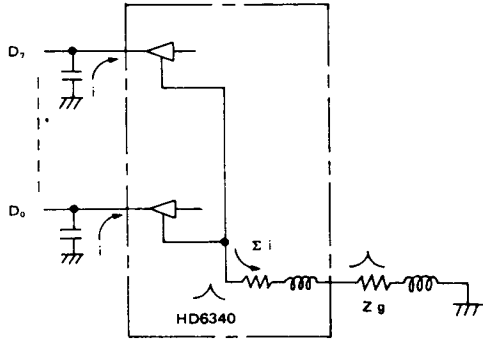
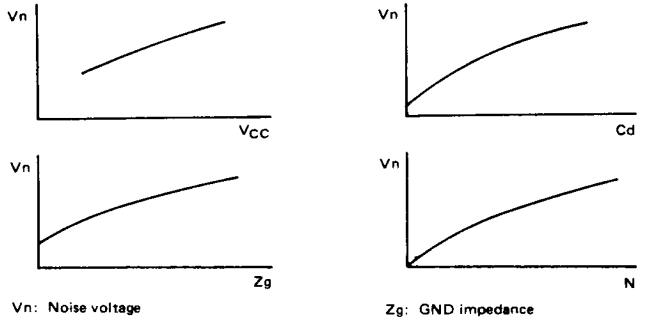


Figure 11 Cause of the Noise



Vn: Noise voltage
Cd: Data bus load capacitance
Zg: GND impedance
N : Number of data bus which changes according to H → L.

Figure 12 The Dependence of the Noise Voltage upon Each Parameter

5

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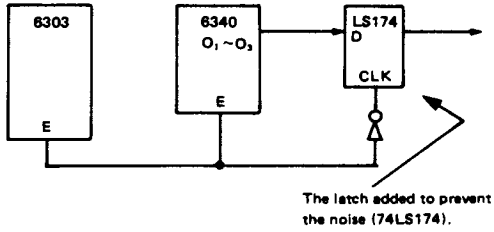
However, it is important to consider the fact that the noise voltage varies according to the type of parameter as indicated in Fig. 12.

(3) Countermeasures

When the noise cause the erroneous operation of the system, the countermeasures to be taken are as follows.

(a) Latch the $O_1 - O_3$ outputs by the falling edge of the signal "E".



The latch added to prevent the noise (74LS174).

■ **Precautions when using Timer 3 (HD6340 only)**

When using the HD63B40P Timer 3 under the conditions

1) external clock mode (CR31 = 0)
2) ÷ 8 prescaler unused (CR30 = 0)

and changing the bits of the control register #3 except for the CR30 bit (e.g. in a case where the interrupt mask bit and O_3 output enable bit are changed and the CR30 is not), there is the possibility that one decrement clock may be omitted.

This phenomenon occurs when t_{DSW} (data setup time; standard spec. 60ns minimum) is less than 80ns, and does not occur when t_{DSW} is greater than 80ns.

Therefore, please avoid to use the HD63B40P in the above status when t_{DSW} is less than 80ns.

(This phenomenon doesn't occur in the HD6340P and HD63A40P.)

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